AN11130

Bias module for 50 V GaN demonstration boards

Rev. 1 — 8 December 2011

Application note

Document information

Info	Content
Keywords	GaN, bias
Abstract	This application note describes a bias controller module for GaN HEMT RF power transistors. It provides constant quiescent drain current with temperature, special bias and power sequencing, and overcurrent protection.

Revision history

Rev	Date	Description
v.1	20111208	initial version

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1. Introduction

GaN HEMT RF power transistors require temperature-compensated gate bias voltages, similar to LDMOS devices, to maintain constant quiescent drain currents with temperature. They are depletion mode devices requiring special bias and power sequencing compared to LDMOS devices. This application note describes a bias controller module which provides these functions, and overcurrent protection.

2. Bias sequencing

The most important consideration for DC with GaN HEMTs, is the bias sequencing. There are two issues to consider:

- Never apply drain voltage when the gate is at 0 V, as the device draws excessive drain current. Thus, any GaN bias controller must include sequenced drain voltage switching.
- For a given V_{GS}, GaN HEMTs are likely to be potentially unstable at lower V_{DS}. Therefore, decrease the gate voltage to below the pinch-off voltage V_P (such as -3 V) while the drain voltage is being turned on and off.

Figure 1 illustrates recommended power-up and power-down sequences for the drain and gate voltages.

(1) The typical discharge time shown is for illustration only, and is not intended as a recommendation. It is important that V_{GS} is held at a voltage of less than V_P until V_{DS} is less than approximately 10 V.

Fig 1. Gate and drain voltage sequence

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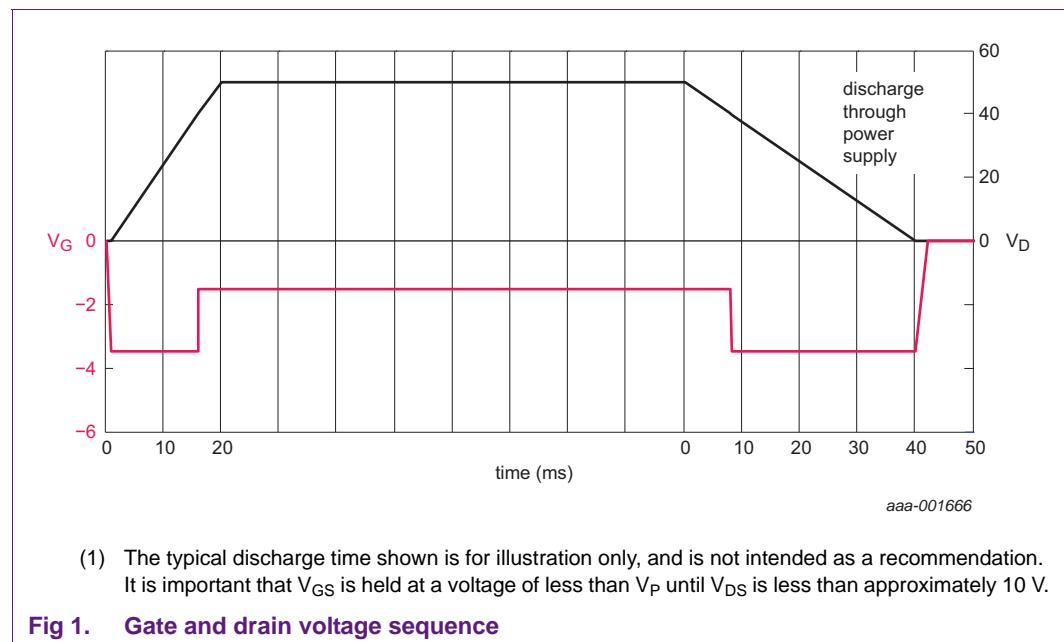
3. Gate current

Because the GaN HEMT gate terminal is a Schottky diode, bias generators must provide significant amounts of both positive and negative gate current:

- GaN HEMTs have higher gate leakage currents than comparable LDMOS devices. The negative gate current can be as high as 500 μA/mm of gate periphery at elevated junction temperatures; the gate current evaluates to -5 mA for a 100 W device operating at 200 $°$C junction temperature.

- When the device is driven into saturation, rectified positive gate current flows into the gate diode. At heavy RF compression, this gate current can exceed 1 mA/mm of gate periphery causing a possible gate current of 30 mA for a 100 W device.

4. Temperature compensation

Similar to LDMOS devices, the gate threshold voltage for GaN devices is approximately proportional to temperature. The gate threshold voltage is the voltage required to maintain a constant quiescent drain current, which for NXP Semiconductors GaN devices, is about +1 mV/$°$C junction temperature. However, practical temperature compensation circuits are obliged to monitor case temperature, where the temperature change is typically only half the junction temperature change. Thus, the bias controller must increase V_{GS} by about +2 mV/$°$C.

5. Summary

The characteristics of the bias controller module described in the following section are summarized in Table 1.

Table 1.   Summary of bias controller characteristics

Drain voltage	12 V to 80 V [1]
Gate voltage	-3 V to -1 V [1]
Gate voltage adjustment range	700 mV typical
Gate voltage temperature compensation	+2 mV/$°$C typical
Gate current, negative	≤ -10 mA
Gate current, positive	≥ 100 mA
Gate voltage ripple	≤ 2 mV (p-p)
Switched drain current	≥ 40 A [2]

[1]   Resistor values may have to be changed for part of range.

[2]   Dependent upon PCB layout.

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6. Circuit description

6.1 Negative voltage generation

The bias controller uses a switched-capacitor voltage inverter, U1, to generate a regulated −4 V from a single positive supply. The +5 V supply is generated from the high-voltage drain supply by linear regulator U4.

U1 operates at a switching frequency of approximately 550 kHz; C3, R4, and C10 are used to reduce output ripple to less than 2 mV (p-p).

When the output voltage is within 5 % of the −4 V set value, the REG output goes LOW. The REG output LOW signal acts as an active-LOW (power valid) signal to enable drain power to the GaN device.
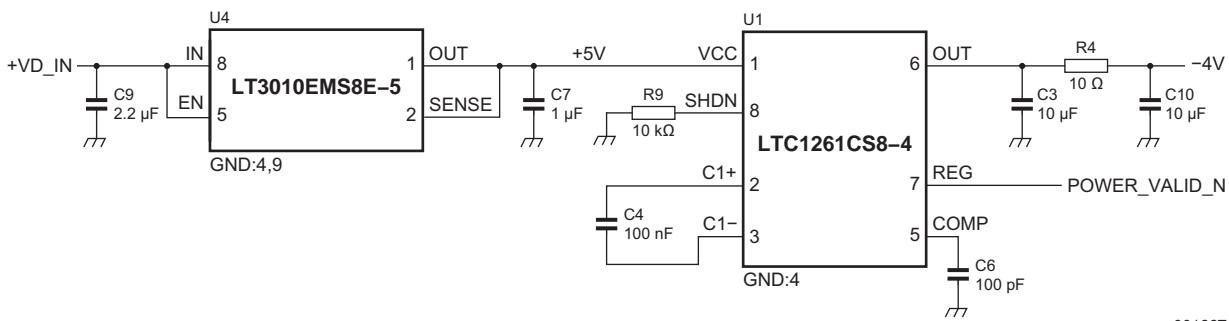
Fig 2. +5 V and −4 V voltage generation circuit

6.2 Drain voltage switching

Most lower power HEMT bias controllers use a P-channel power MOSFET as the drain voltage load switch. This has the advantage of simplicity, often requiring nothing more than level-shifting transistors between the voltage inverter 'power valid' signal and the MOSFET gate. However, as load currents increase above 2 A to 5 A, the required MOSFET becomes large and expensive. Consequently, this bias controller uses a common hot-swap controller IC, U2 to drive an inexpensive N-channel MOSFET.

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Fig 3.   Drain voltage load switch circuit
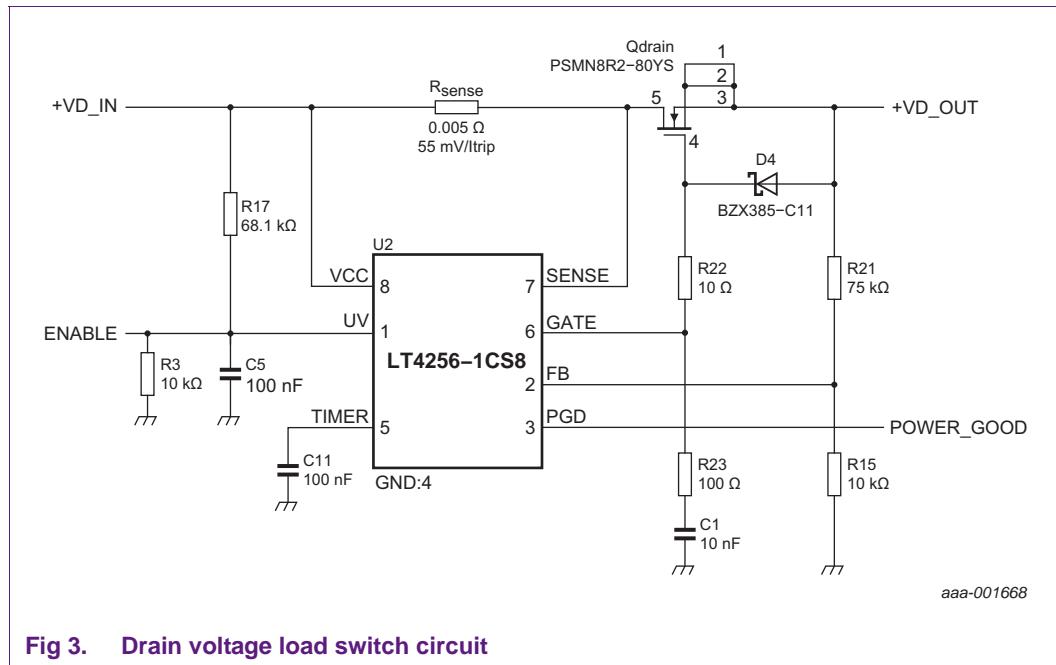
U2 contains an internal charge pump for driving the gate of the external N-channel MOSFET, Qdrain. It also includes a programmable ramp-up rate, and optional overcurrent fault detection and foldback current limiting. If the voltage drop across sense resistor Rsense exceeds 55 mV, U2 disconnects power from the drain, and leaves it latched off until power is cycled.

Qdrain is a low-cost high-density TrenchMOS device in a small power SO8 package. It has a typical on-resistance of less than 10 mΩ and a drain current limit of more than 80 A.

6.3 Temperature compensation

The bias controller uses a small-signal PNP transistor (mounted in contact with the baseplate) to monitor temperature and generate a +8 mV/°C compensating voltage.



Fig 4.   Temperature compensating circuit

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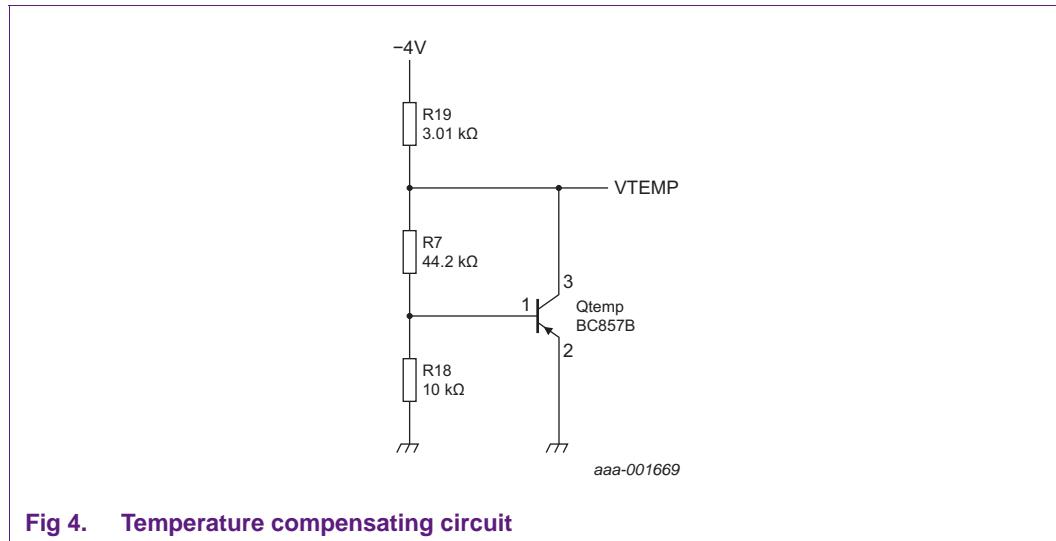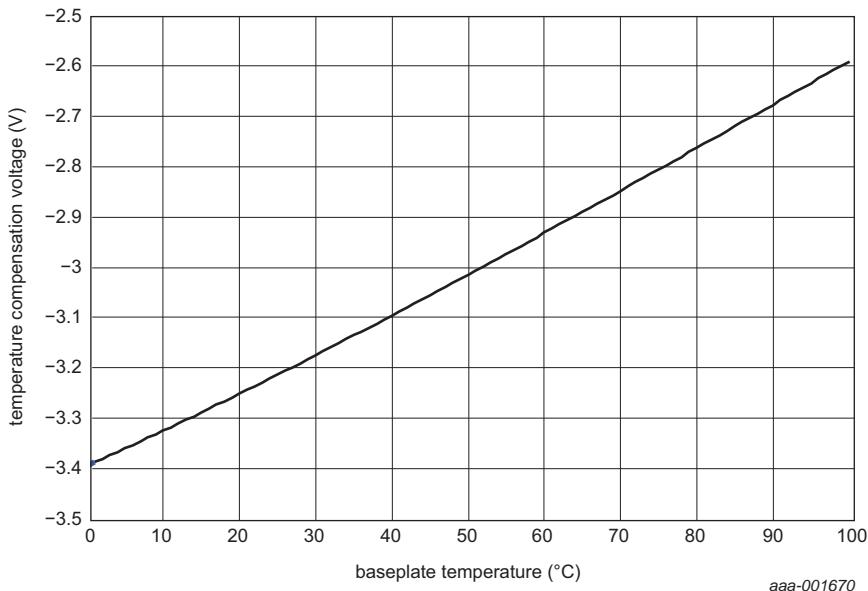
Fig 5. Temperature compensating voltage

6.4 Gate voltage adjustment

A variable voltage derived from the −4 V supply is summed with the temperature monitor voltage to generate a temperature-compensated gate voltage. R13 and R14 are selected to set the desired gate voltage trim range, and R6 is selected to provide the desired amount of temperature compensation. Figure 6 shows typical values for V_{GS} = −1.6 V.

U3 is a dual rail-to-rail high-current operational amplifier chosen because it is stable into any capacitive load. It can deliver more than 100 mA of output current to meet the positive gate current requirements of most GaN HEMTs.

Fig 6. Gate voltage adjustment circuit

Fig 7. Gate voltage
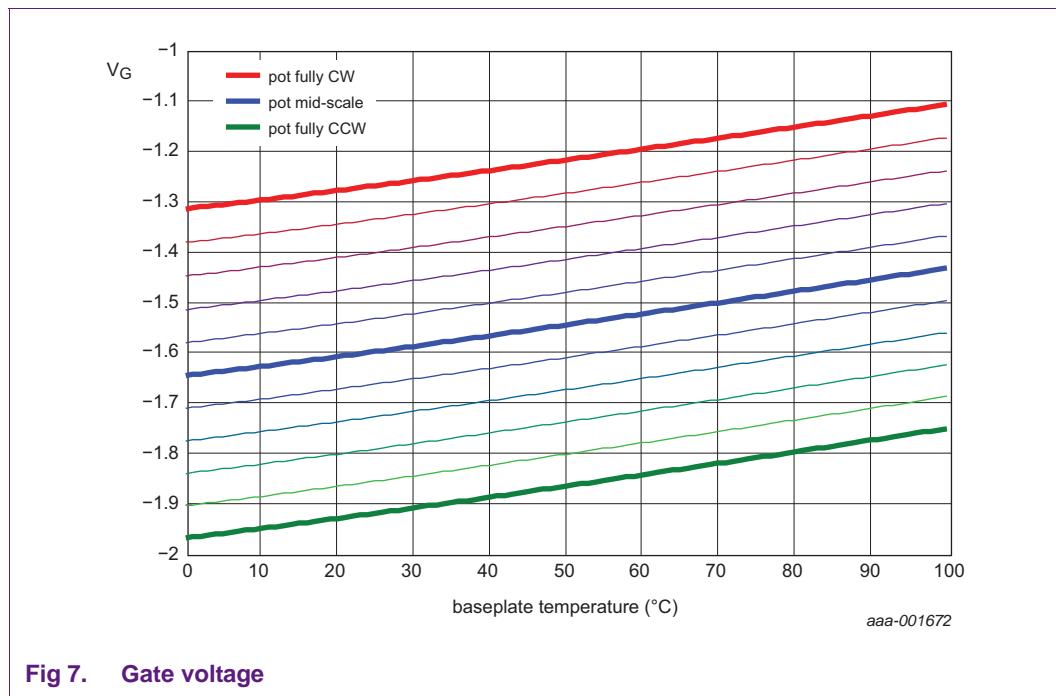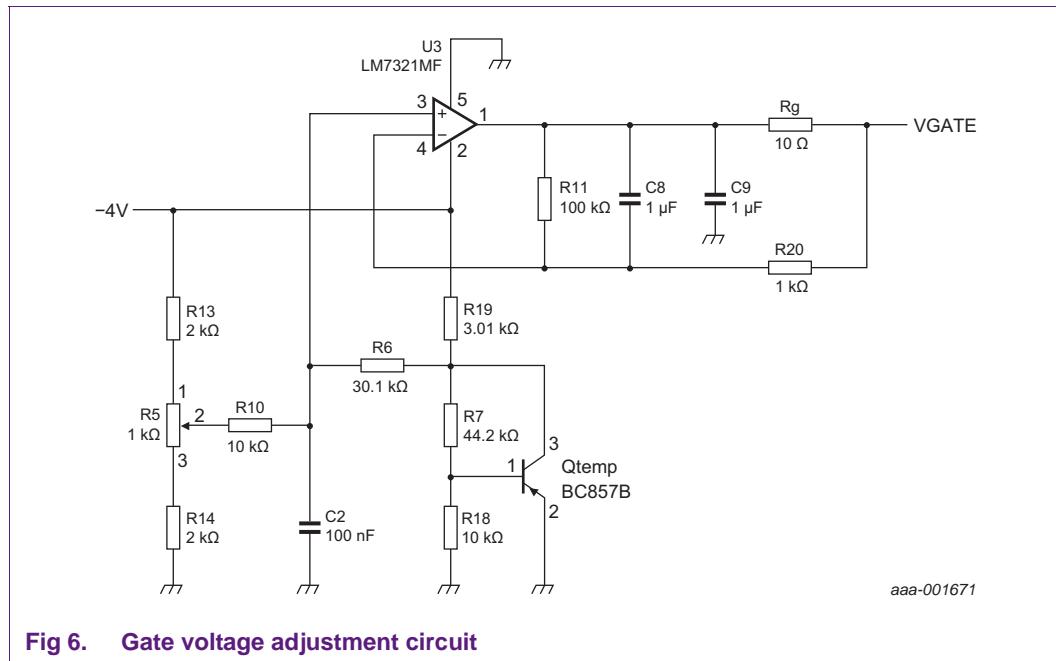
The output impedance of the bias source is low (less than 1 Ω) because of the feedback around operational amplifier U3. However, HEMT applications usually require a series gate resistor of 5 Ω to 20 Ω, instead of a bias inductor, to ensure low-frequency device stability.

Because the GaN HEMT quiescent gate current can increase at high temperatures, a significant voltage drop can be developed across this gate resistor, increasing V_{GS} by 200 mV or more. This can be a serious problem because the increased gate voltage can push the HEMT operating point into a region of instability or even cause thermal runaway.

One solution is to provide DC feedback from the HEMT gate terminal to the operational amplifier inverting input, allowing it to compensate for voltage dropped across gate resistor Rg. Feedback through R20 compensates for voltage dropped across Rg. To minimize RF non-linearity and memory effects, make sure that $1 / (R20 \times C8)$ is less than the lowest modulation frequency of the RF signal.

6.5 Resistor value selection

The resistor values in the schematic are for a 50 V device with a nominal V_{GS} of −2.1 V, +2 mV/°C V_{GS} temperature coefficient, and 11 A I_{DS} overcurrent sense. Other nominal operating conditions may require resistor value changes:

- R17 determines the supply voltage at which the drain is connected.
  R17 = R3 $(V_D / 4 − 1)$, so V_D = 31 V with the 68.1 kΩ value in the design.

- R21 determines the supply voltage at which operating V_{GS} is applied.
  R21 = R15 $(V_D / 4.45 − 1)$, so V_D(good) = 38 V with the 75.0 kΩ value in the design.

- Rsense determines the foldback current limit. I_{LIMIT} = 0.055 / Rsense, so I_{LIMIT} = 11 A with the 5 mΩ value in the design.

6.6 Full schematic

The complete schematic of the bias controller combines the preceding subcircuits with 'glue circuitry' and several (possibly optional) additional convenience features.

- LEDs D1 and D2 provide visual indication of valid gate and drain voltages.

- Switch S1 allows the GaN amplifier to be placed easily in 'standby', where the nominal gate voltages are applied, but drain power is disconnected.

- When S1 is set to 'Vd on' and the drain supply is not fully on (ramping up or down), diode D3 and MOSFET Q3 turn on MOSFET Q2, pulling the gate voltage down to −4 V.

Table 2.   Bias module bill of materials

Component	Description	Value	Remarks
C9, C12	capacitor, 100 V 10 % X7R, 1206	1 μF	
C7, C8	capacitor, 50 V 10 % X7R, 0805	1 μF	
C2, C4, C5, C11	capacitor, 50 V 10 % X7R, 0805	100 nF	
C6	capacitor, 50 V 5 % NP0, 0805	100 pF	
C3, C10	capacitor, 10 V 20 % X7R, 0805	10 μF	
C1	capacitor, 50 V 10 % X7R, 0805	10 nF	
D1	LED, green, 0805		
D2	LED, yellow, 0805		
D4	diode, Zener 11 V 300 mW		NXP BZX385-C11
D3	dual diode, common-cathode		NXP BAV74
L1	ferrite bead, 200 mA, 0805	1000 mH?	
Q1, Q2, Q4	transistor, N-ch MOS 30 V 0.8 A		NXP BSH103
Q3	transistor, P-ch MOS 30 V 0.8 A		NXP BSS84
R13, R14	resistor, 1 % 100 ppm CF, 0805	2.00 kΩ	
R5	potentiometer, 5t cermet	1 kΩ	

Table 2. **Bias module bill of materials**

Component	Description	Value	Remarks
R19	resistor, 1 % 100 ppm CF, 0805	3.01 kΩ	
R7	resistor, 1 % 100 ppm CF, 0805	44.2 kΩ	
R3, R9, R10, R12, R15, R16, R18	resistor, 1 % 100 ppm CF, 0805	10.0 kΩ	
R6	resistor, 1 % 100 ppm CF, 0805	30.1 kΩ	
R4, R22, R24	resistor, 1 % 100 ppm CF, 0805	10.0 kΩ	
R1, R8, R20	resistor, 1 % 100 ppm CF, 0805	1.00 kΩ	
R17	resistor, 1 % 100 ppm CF, 0805	68.1 kΩ	
R23	resistor, 1 % 100 ppm CF, 0805	100 kΩ	
R2, R11	resistor, 1 % 100 ppm CF, 0805	100 kΩ	
R21	resistor, 1 % 100 ppm CF, 0805	75.0 kΩ	
S1	switch, SPDT right-angle SMD		Tyco 1437575-1
U4	voltage regulator, 5 V 100 mA		Linear LT3010EMS8E-5
U1	switching capacitor inverter		Linear LTC1261CS8-4
U2	hot swap controller		Linear LT4256-1CS8
U3	rail-rail opamp		National LM7321MF

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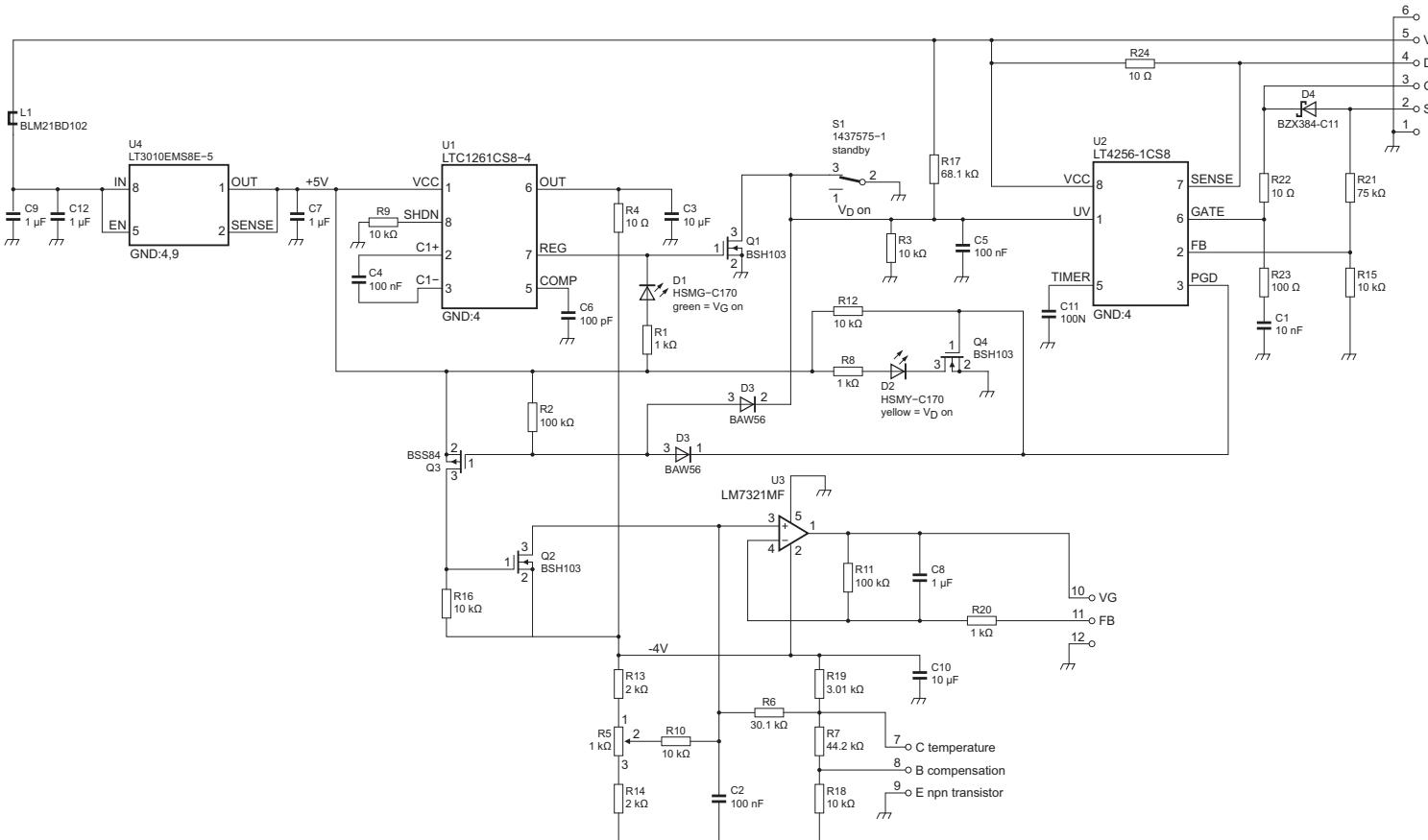
Fig 8.   Bias module schematic

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7. PCB layout
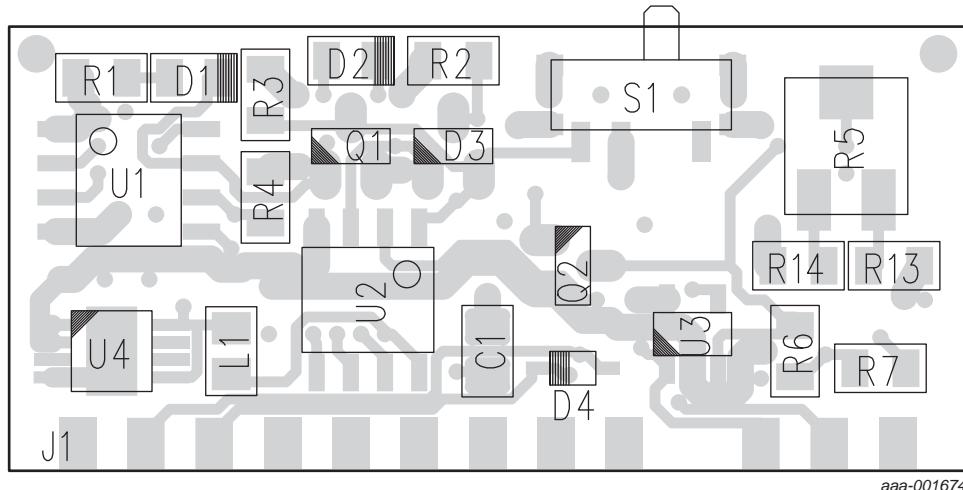
Fig 9.   PCB top-side layout
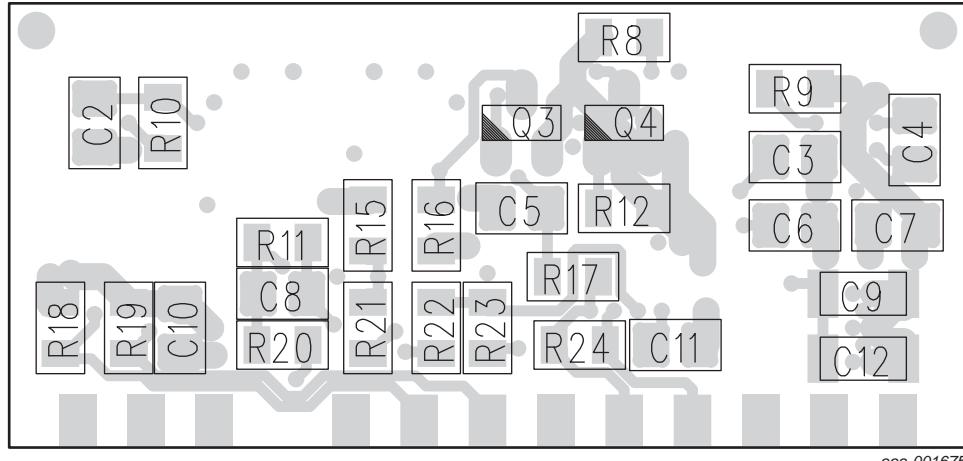
Fig 10.   PCB bottom-side layout

8. Abbreviations

Table 3.   Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

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